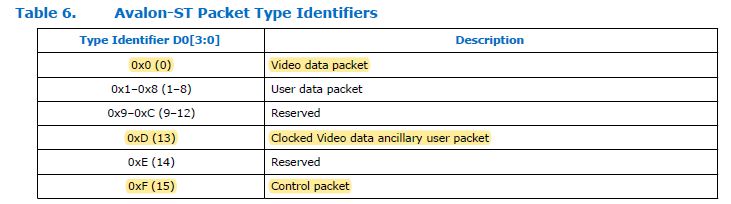
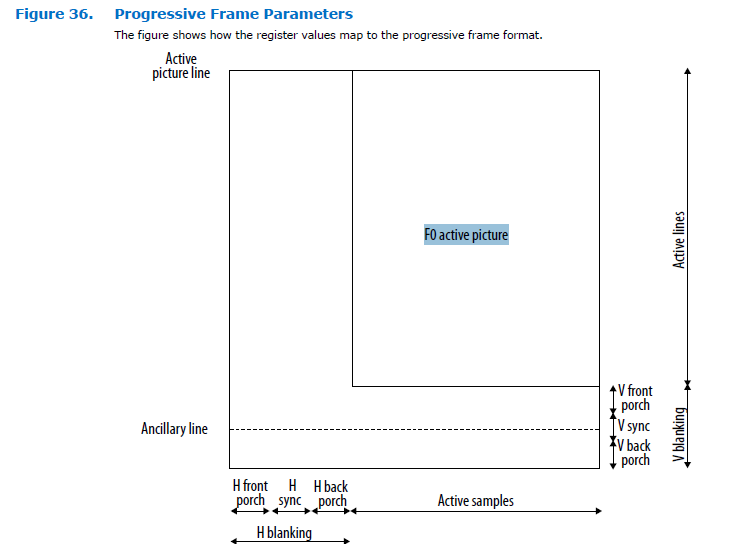
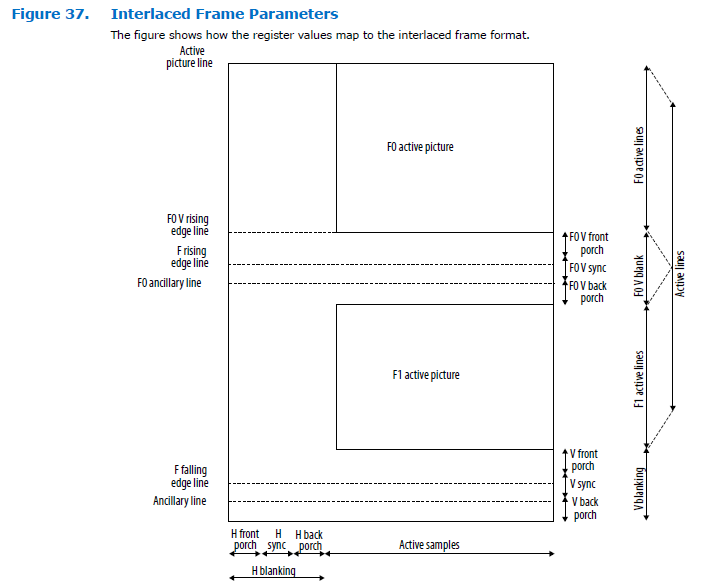
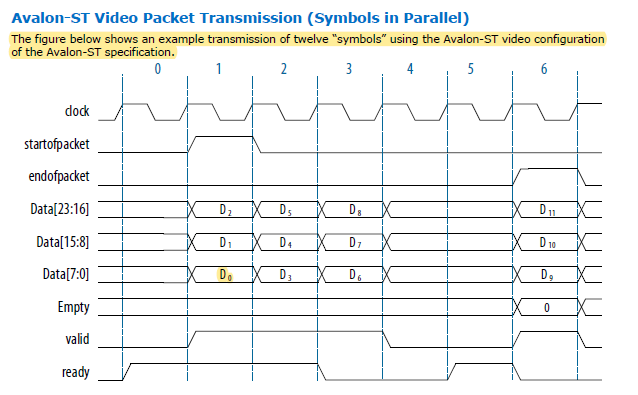
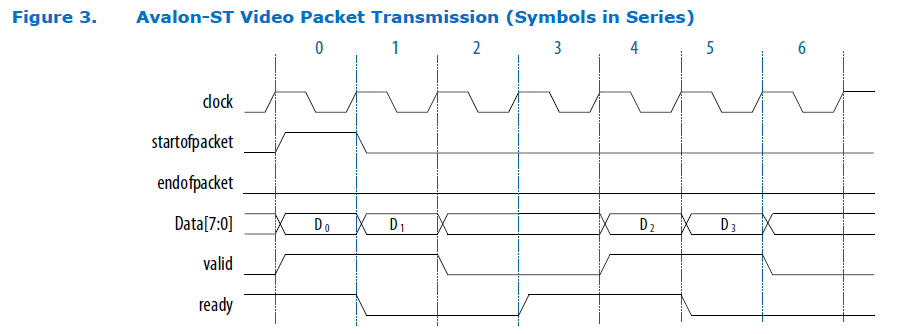
**Part 1. ug\_vip Control Packet**



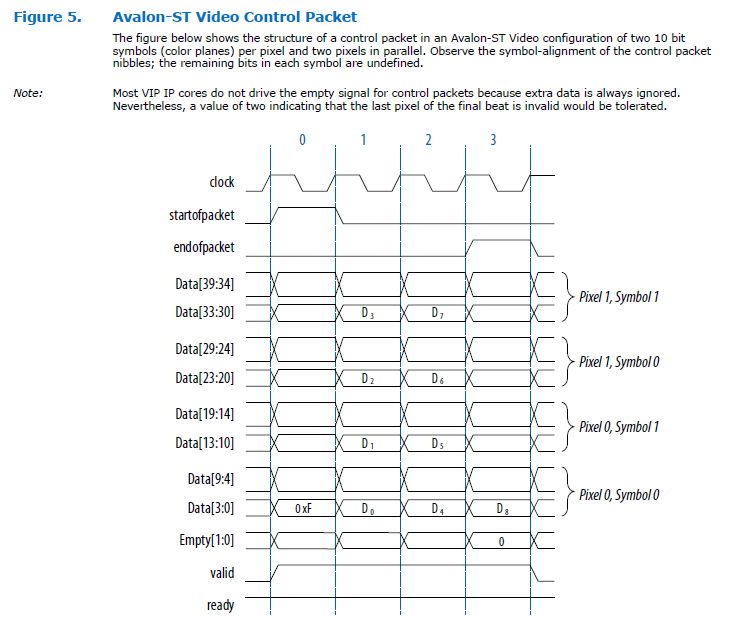


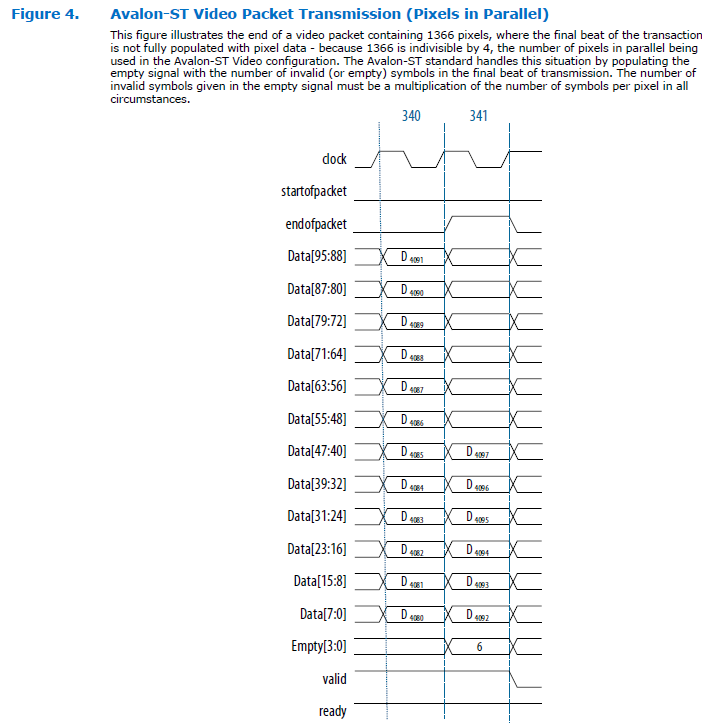


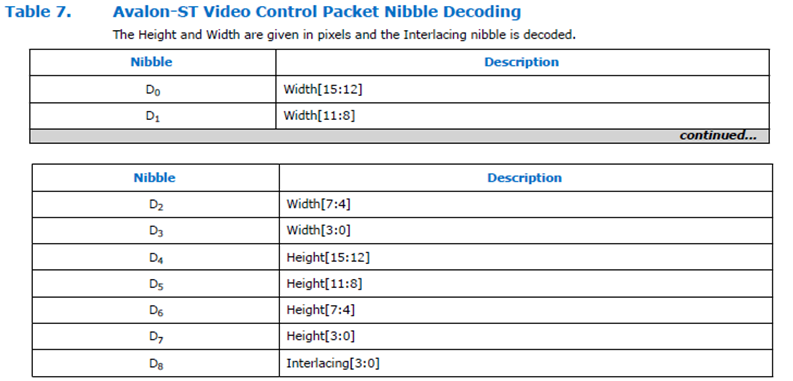




Avalon-ST Video Control Packet Nibble Decoding:

1. Avalon-ST Data : 40bit ,示意圖





Avalon-ST Data : 24bit , 下圖為rgb8\_8\_8示意圖

Control Packet. RGB 8:8:8

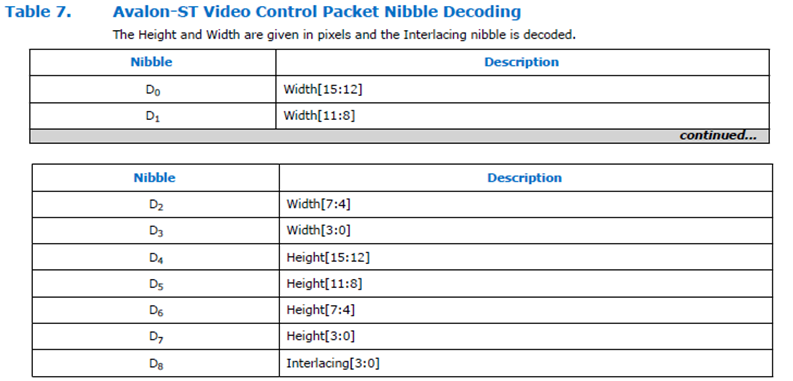
Avalon-ST Data : 24bit ,

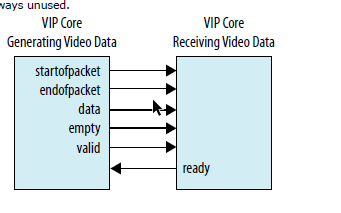
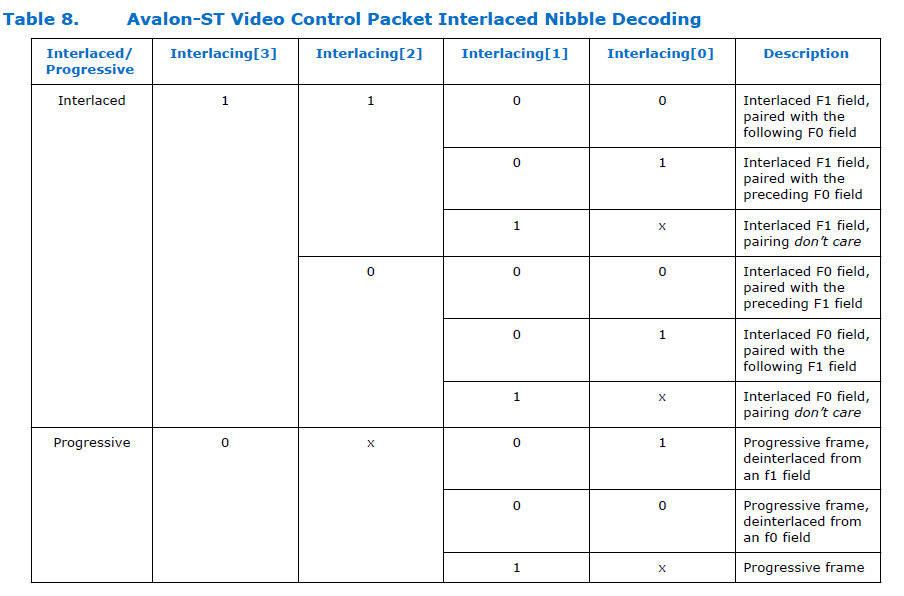
bit per symbol: 8

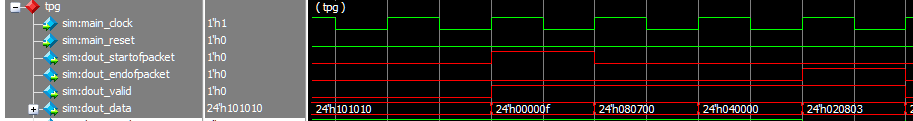
bit per color sample: 8,

symbol in parallel : 3

symbol in sequence: 1







0xF : control packet

|  |  |  |
| --- | --- | --- |
| **第一個橘色框**  D0: 4’h0 Width[15:12]  D1: 4’h7 Width[11:8]  D2: 4’h8 Width[7:4] | **第二個黃色框**  D3: 4’h0 Width[3:0]  D4: 4’h0 Height[15:12]  D5: 4’h4 Height[11:8] | **第三個淡橘色框**  D6: 4’h3 Height[7:4]  D7: 4’h8 Height[3:0]  D8: 4’h2 Interlacing[3:0]  Interlacing 🡺 table 8. Progress frame |

**\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*結論\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\***

**此封包定義的**

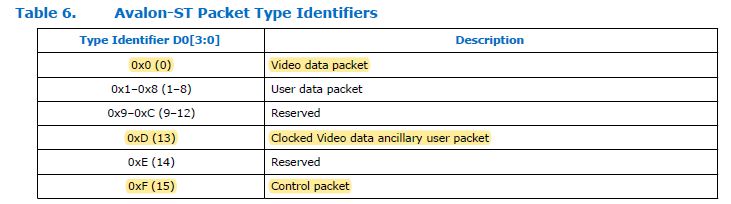
**Width: 16’h0780 (1920)**

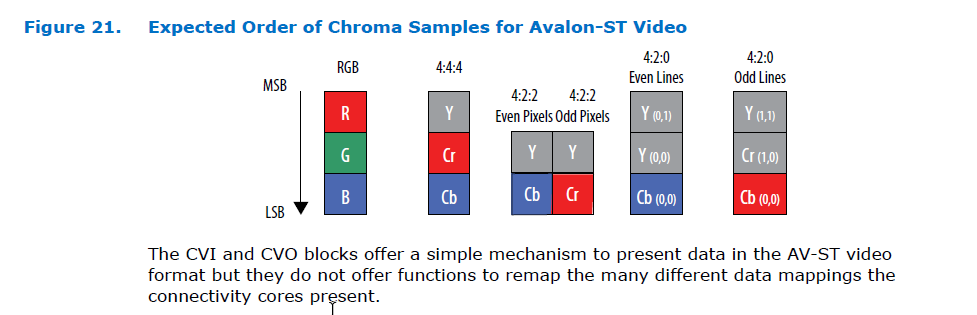
**Height: 16’h0438(1080)**

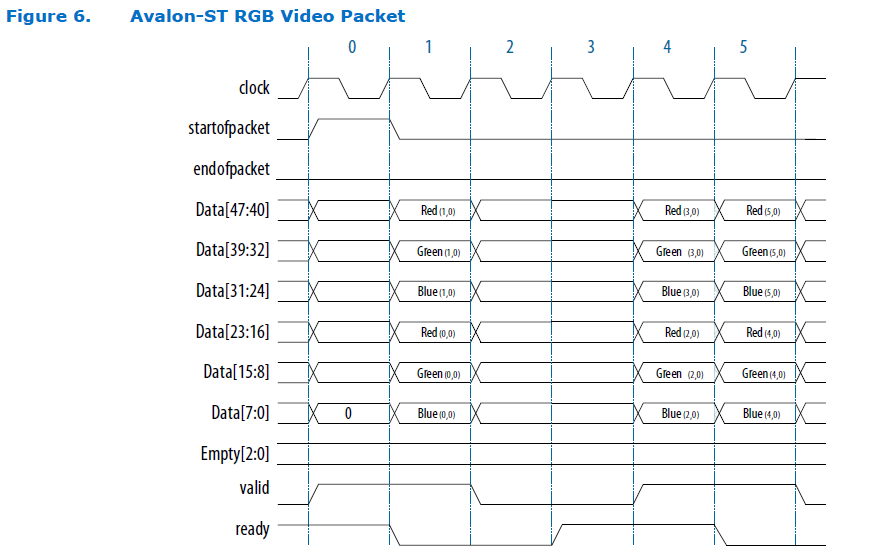
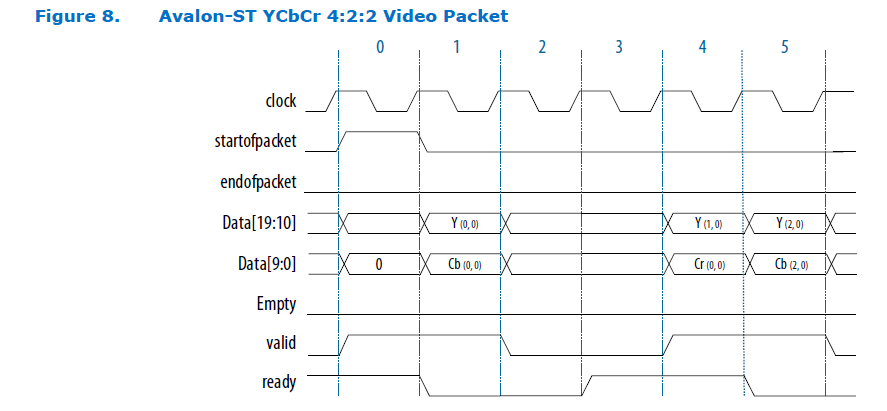
**Interlacing: 4’h2**

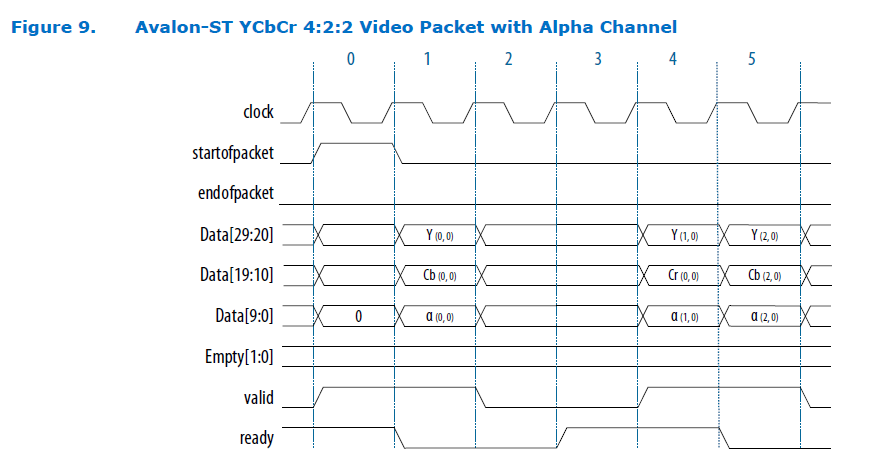
**\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\***

**Part 2. ug\_vip Video Packet**









1. 每一張frame 開始前會送一次 sop + control packet + eop
2. Sop+ lane 0 + eop +lane 1 + eop + lane 2 + …… last of lane + eop
3. sop + control packet + eop
4. Sop+ lane 0 + eop +lane 1 + eop + lane 2 + …… last of lane + eop

.

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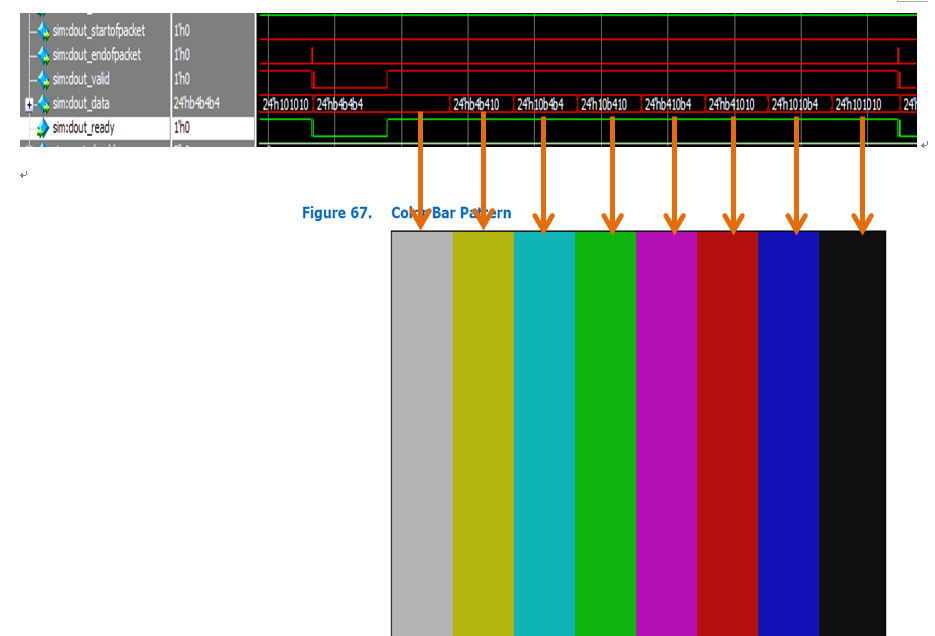
.

下圖為 video packet 24bit

data: 7:0 🡺 Blue 分量

data: 15:8 🡺 Green分量

data: 23:16 🡺 Red 分量



***Reference Website:*** [***https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug\_vip.pdf***](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_vip.pdf)